

Fig. 1

FIG. 1

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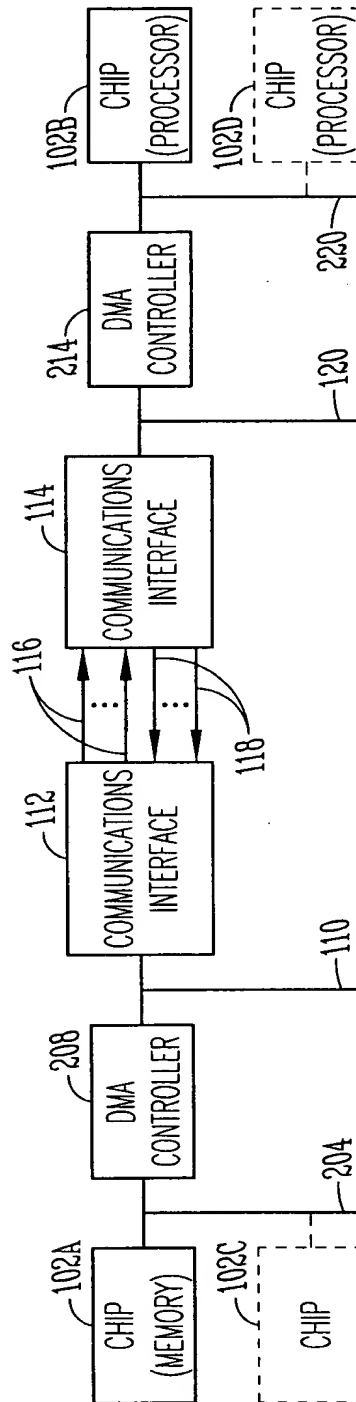


Fig. 2

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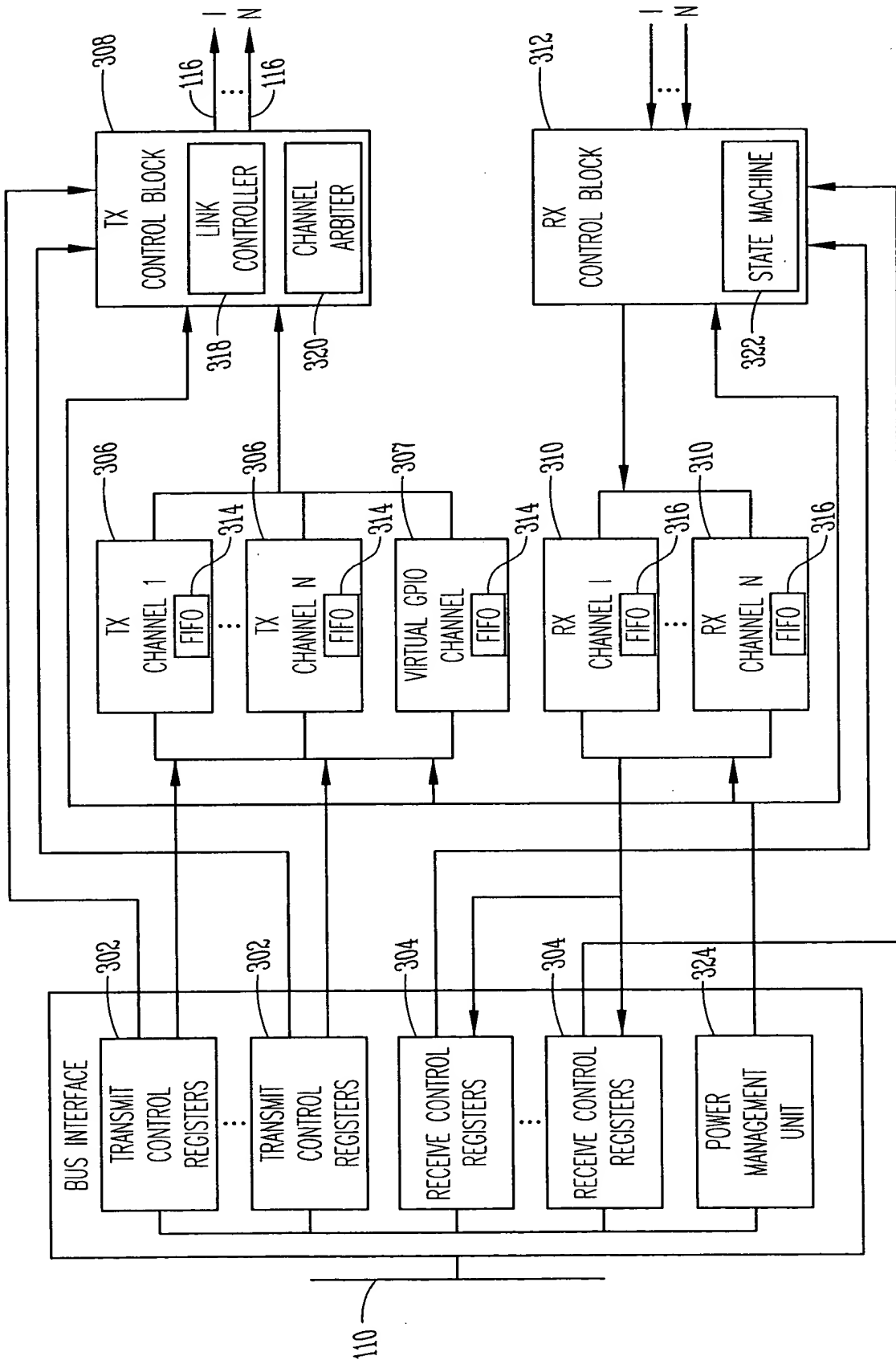


Fig. 3

FIG. 3

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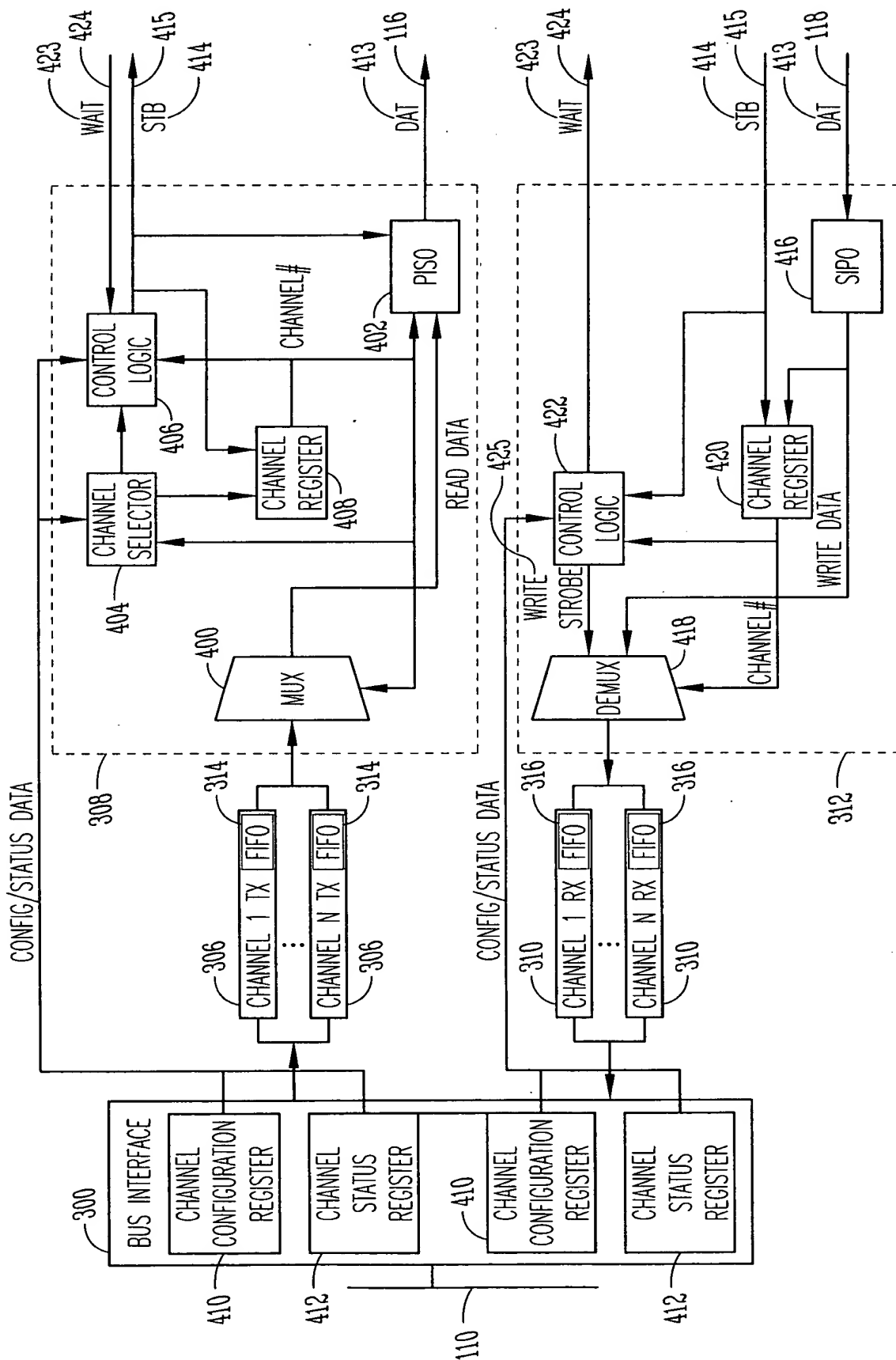


Fig. 4

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FIG. 5

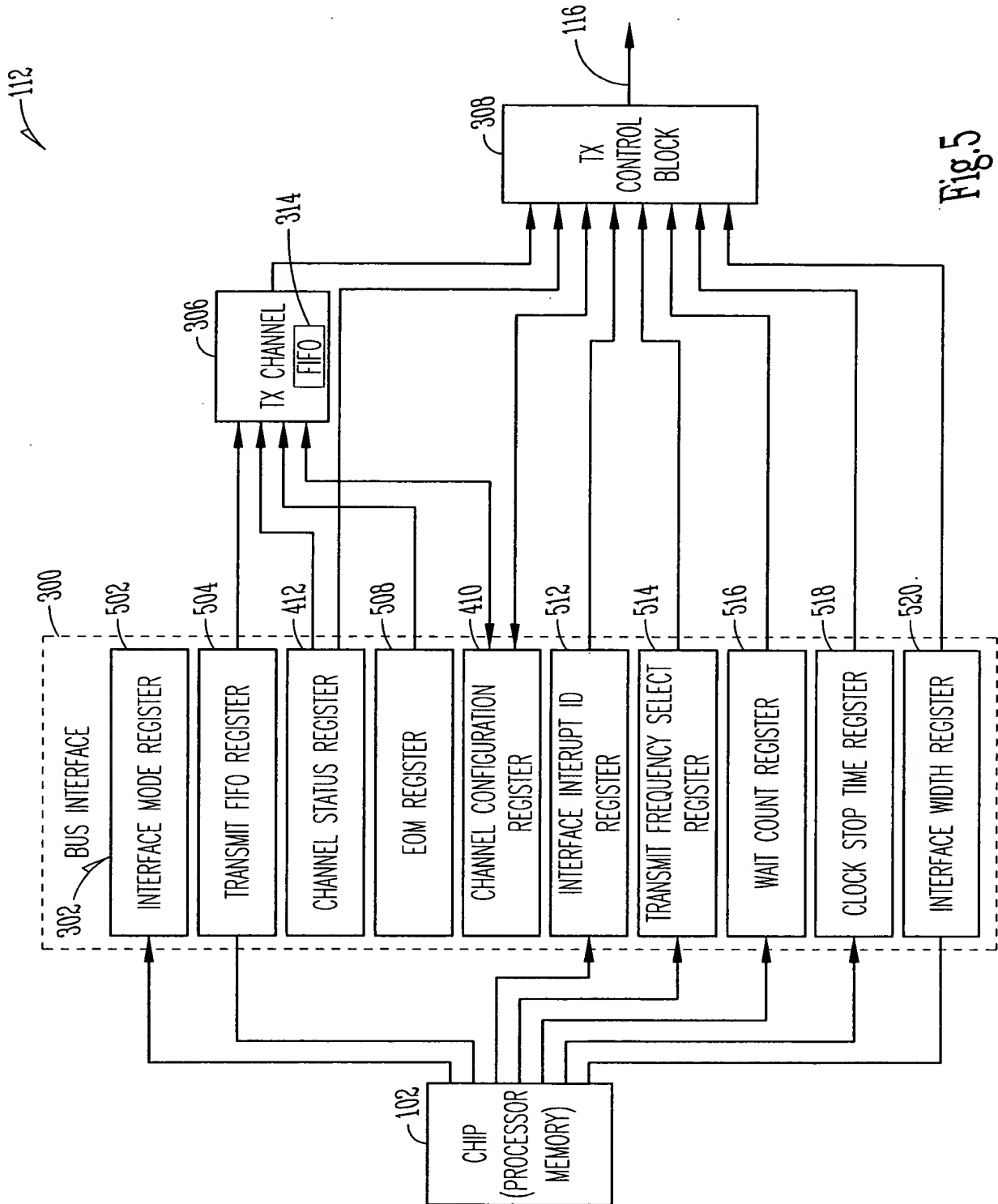


Fig.5

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CHANNEL STATUS REGISTER BIT LAYOUT AND DEFINITIONS			
BITS	ACCESS	NAME	DESCRIPTION
31:26	N/A	RESERVED	RESERVED
602 25	READ	RxEOM	RECEIVE CHANNEL RECIEVED EOM • 0=CHANNEL DID NOT RECIEVE EOM • 1=CHANNEL RECIEVED EOM
604 24	READ	RxWAIT	RECEIVE CHANNEL IN WAIT STATE • 0=CHANNEL NOT IN WAIT STATE • 1=CHANNEL IN WAIT STATE
606 23	READ	RxEMPTY	RECEIVE FIFO EMPTY • 0=NOT EMPTY • 1=EMPTY
608 22	READ	RxFULL	RECEIVE FIFO FULL • 0=NOT FULL • 1=FULL
610 21:16	READ	RxFULLNESS	FULLNESS OF RECEIVE FIFO • 000000=FIFO IS EITHER FULL OR EMPTY (SEE RxFULL AND RxEMPTY BITS) • NONZERO=NUMBER OF BYTES OF DATA IN RECEIVE FIFO
15:9	N/A	RESERVED	RESERVED
604 8	READ	TxWAIT	TRANSMIT CHANNEL IN WAIT STATE • 0=CHANNEL NOT IN WAIT STATE • 1=CHANNEL IN WAIT STATE
606 7	READ	TxEMPTY	TRANSMIT FIFO EMPTY • 0=NOT EMPTY • 1=EMPTY
608 6	READ	TxFULL	TRANSMIT FIFO FULL • 0=NOT FULL • 1=FULL
610 5:0	READ	TxFULLNESS	FULLNESS OF TRANSMIT FIFO • 000000=FIFO IS EITHER FULL OR EMPTY (SEE TxFULL AND TxEMPTY BITS) • NONZERO=NUMBER OF BYTES OF DATA IN TRANSMIT FIFO

Fig.6

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CHANNEL CONFIGURATION REGISTER BIT LAYOUT AND DEFINITIONS			
BITS	ACCESS	NAME	DESCRIPTION
31:26	N/A	RESERVED	RESERVED
25:24	READ/WRITE	EOCSERVICE	EARLY EOC SERVICE SELECT • 00=NONE • 01=INTERRUPT • 1x=RESERVED
23:21	READ/WRITE	RxSERVICE	RECEIVE FIFO SERVICE SELECT • 000=NONE • 001=DMA • 010=INTERRUPT • 011=RESERVED • 1XX=RESERVED
20:19	READ/WRITE	RxTHRESH- LEVEL	RECEIVE FIFO SERVICE THRESHOLD • 00=4 BYTES • 01=8 BYTES • 10=16 BYTES • 11=32 BYTES
18	READ/WRITE	RxDfC ENABLE	DIRECT FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
17	READ/WRITE	RxMfC ENABLE	MESSAGE FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
16	READ/WRITE	RxENABLE	RECEIVE FIFO CHANNEL ENABLE • 0=CHANNEL DISABLED • 1=CHANNEL ENABLED
15:11	READ/WRITE	RESERVED	RESERVED
10:8	READ/WRITE	TxBLOCK	TRANSMIT BLOCK SIZE • 000=4 BYTES • 001=8 BYTES • 010=16 BYTES • 011=32 BYTES • 1XX=RESERVED
7:5	READ/WRITE	TxSERVICE	TRANSMIT FIFO SERVICE SELECT • 000=NONE • 001=DMA • 010=INTERRUPT • 011=RESERVED • 1XX=RESERVED
4:3	READ/WRITE	TxTHRESH- LEVEL	TRANSMIT FIFO SERVICE THRESHOLD • 00=4 BYTES • 01=8 BYTES • 10=16 BYTES • 11=32 BYTES
2	READ/WRITE	TxDfCENABLE	DIRECT FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
1	READ/WRITE	TxMfCENABLE	MESSAGE FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
0	READ/WRITE	TxENABLE	TRANSMIT FIFO CHANNEL ENABLE • 0=CHANNEL DISABLED • 1=CHANNEL ENABLED

Fig.7

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INTERFACE INTERRUPT IDENTIFICATION REGISTER			
BITS	ACCESS	NAME	DESCRIPTION
31:24	N/A	RESERVED	RESERVED
23:17	READ/WRITE 1 TO CLEAR	TX_INTx	TRANSMIT FIFO INTERRUPT FOR CHANNEL x
16	N/A	RESERVED	RESERVED
15:9	READ/WRITE 1 TO CLEAR	EOC_INTx	EOC INTERRUPT FOR CHANNEL x
8	N/A	RESERVED	RESERVED
7:1	READ/WRITE 1 TO CLEAR	RX_INTx	RECEIVE FIFO INTERRUPT FOR CHANNEL x
0	READ/WRITE 1 TO CLEAR	VGPI0_INT	VGPI0 INTERRUPT – SEE BBVGED REGISTER FOR WHICH VGPI0 PIN

Fig.8

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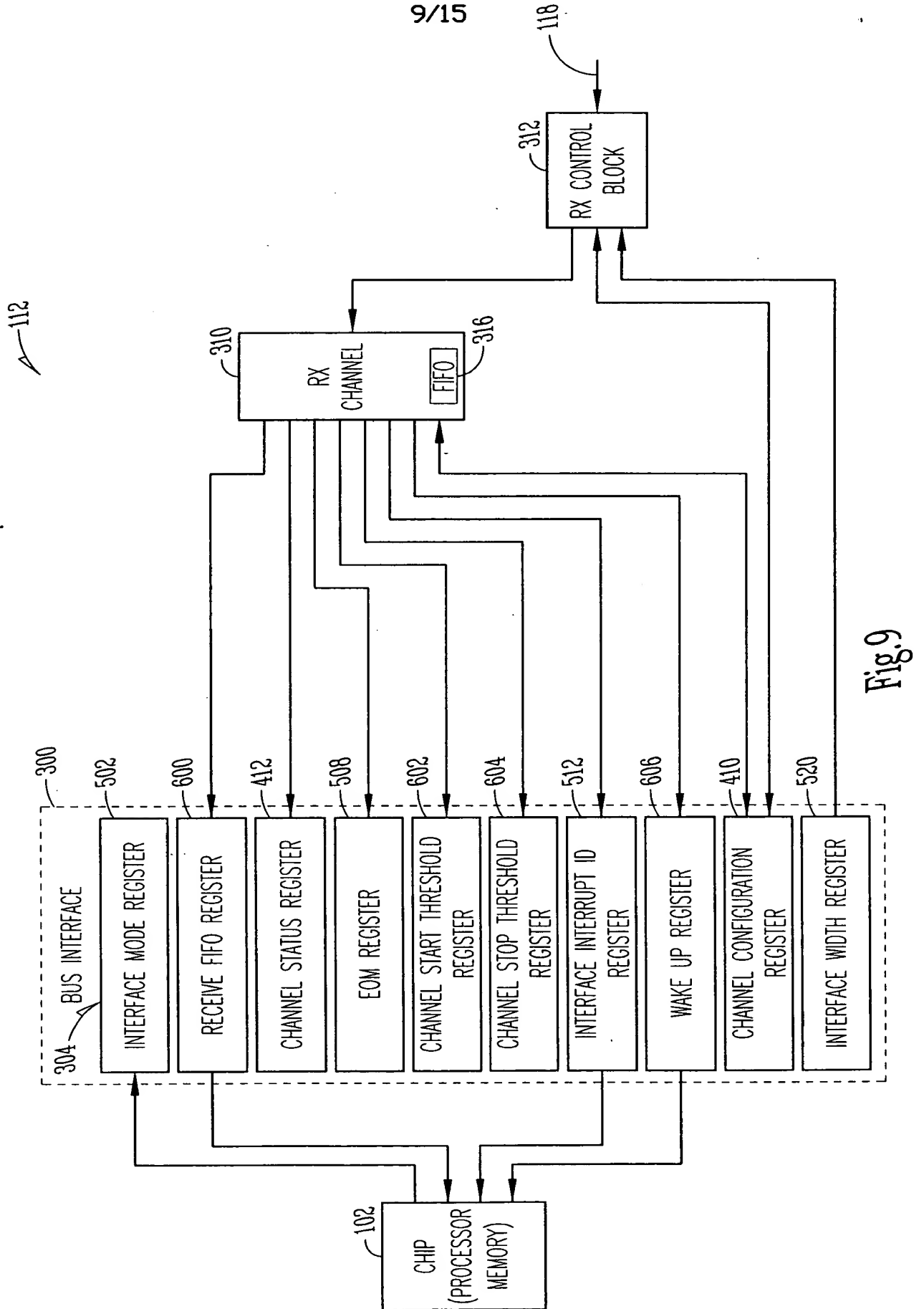


Fig. 9

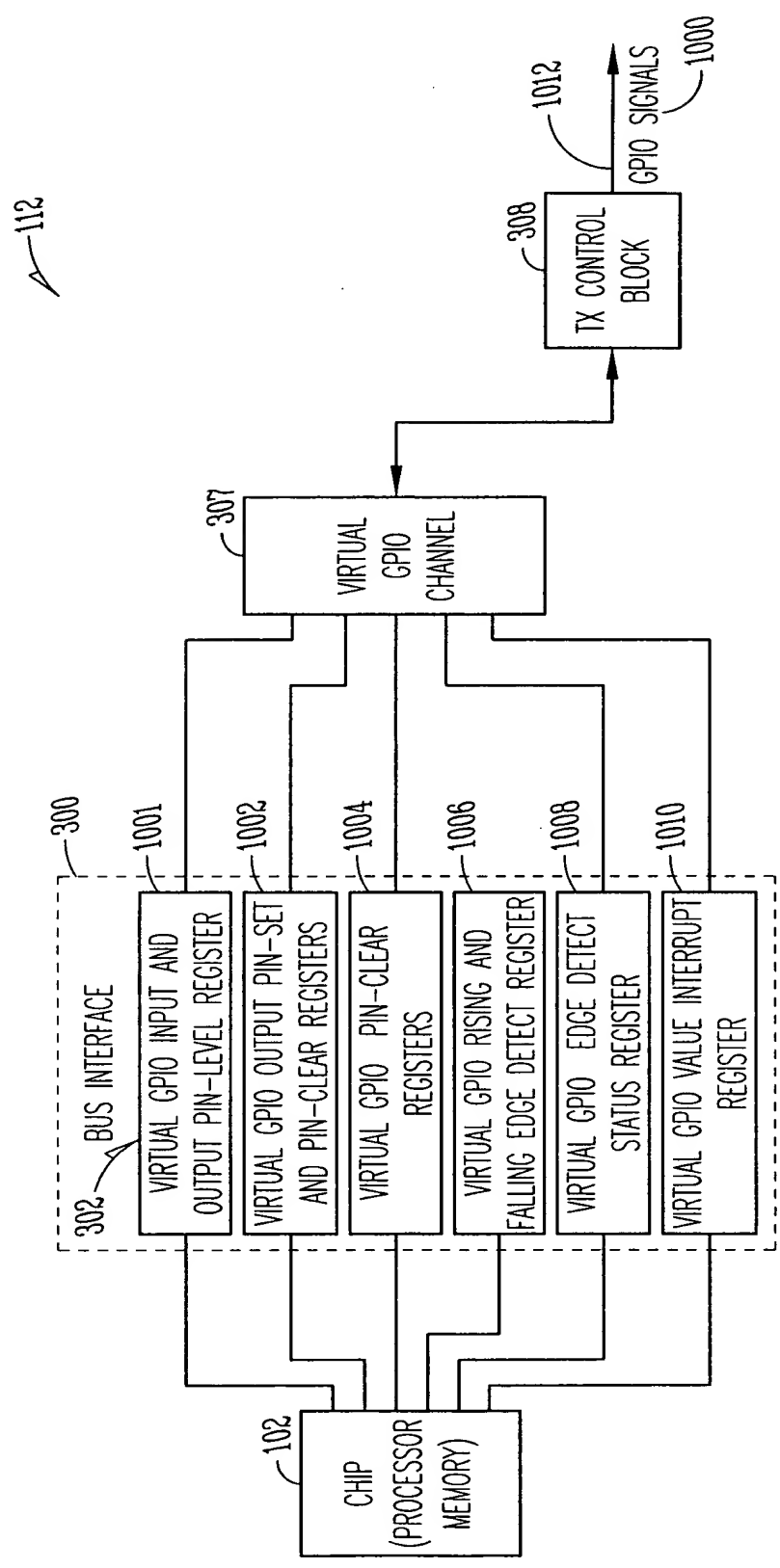


Fig.10

FIG. 10

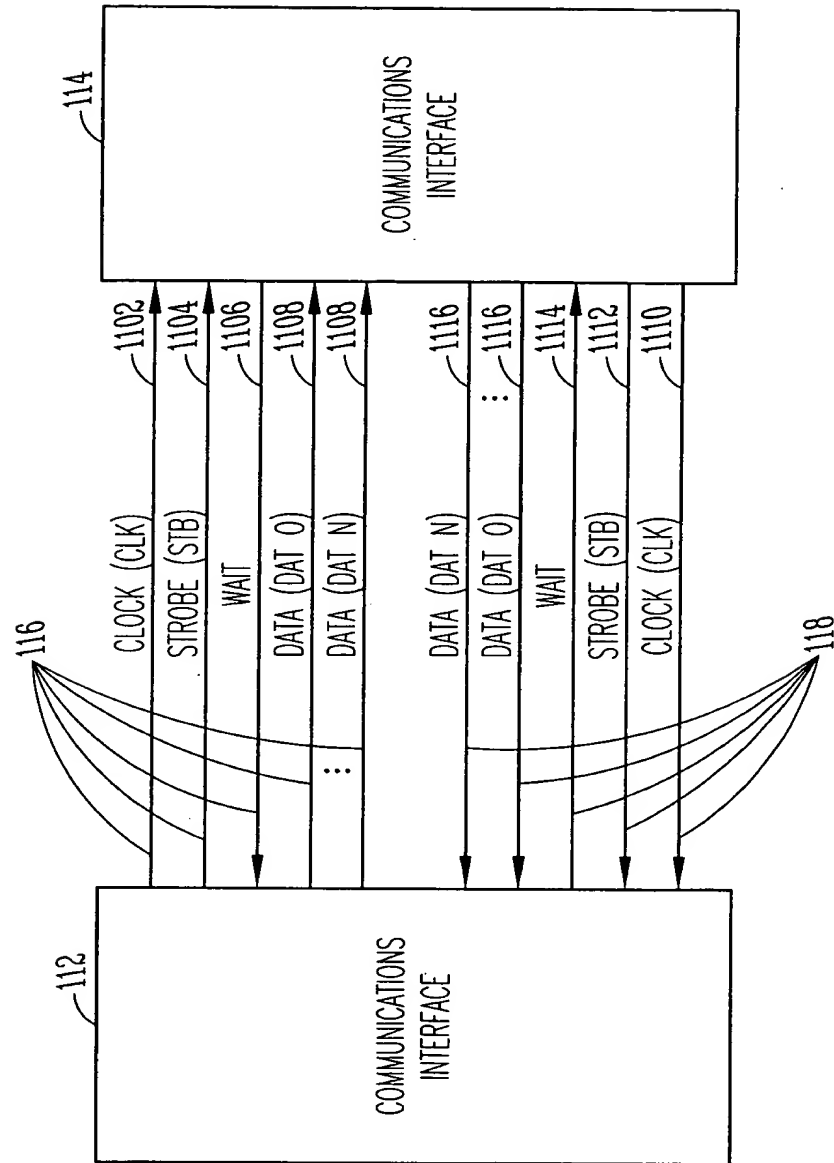


Fig.11

FIG. 11

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CHANNEL NUMBER	DESCRIPTION
0	NULL CHANNEL TO SIGNAL EOM
1	DATA CHANNEL 1
2	DATA CHANNEL 2
3	DATA CHANNEL 3
4	DATA CHANNEL 4
5	DATA CHANNEL 5
6	DATA CHANNEL 6
7	DATA CHANNEL 7
8	RESERVED
9	RESERVED
10 (A)	RESERVED
11 (B)	EMPTY CHANNEL
12 (C)	WAKE UP CHANNEL
13 (D)	VITTUAL GPIO CHANNEL
14 (E)	STOP MESSAGE CHANNEL
15 (F)	START MESSAGE CHANNEL

Fig.12

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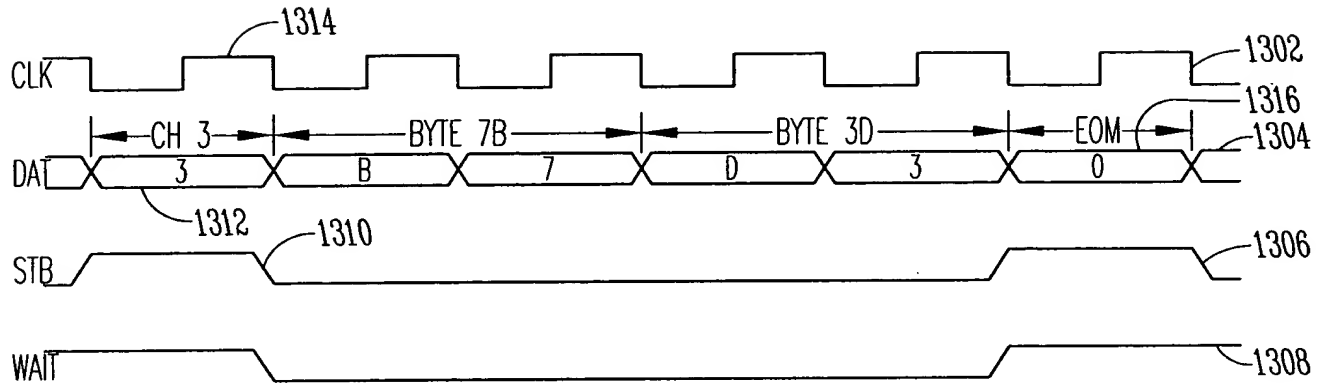


Fig.13

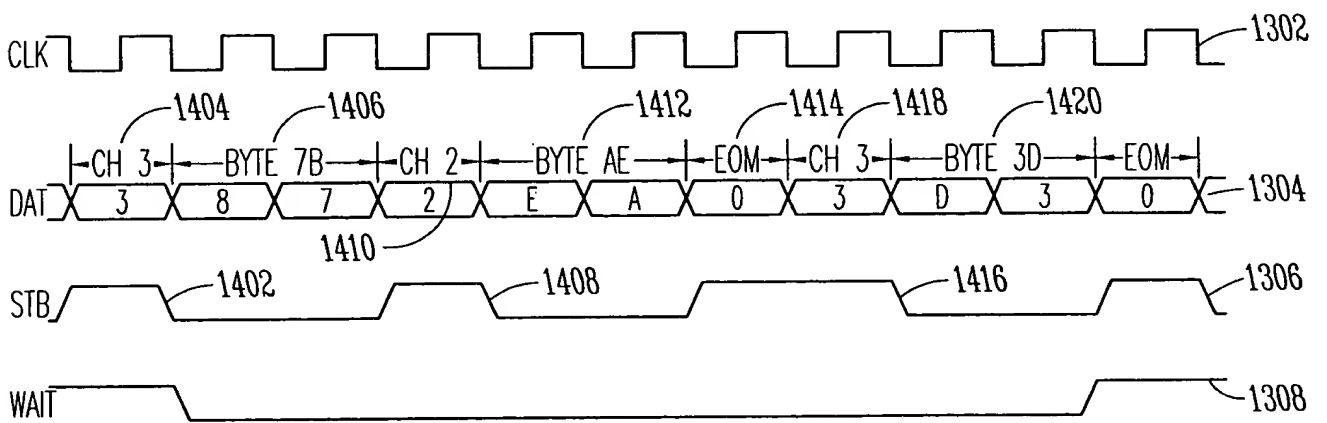


Fig.14

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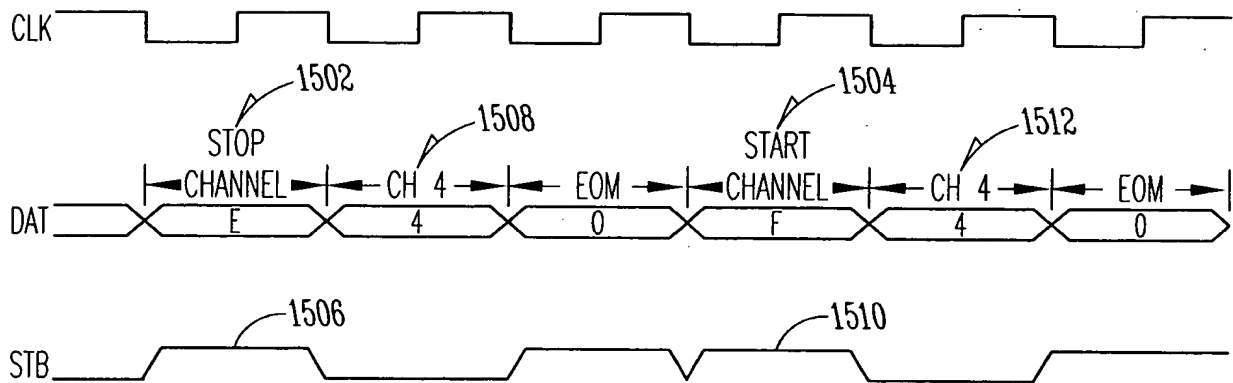


Fig.15

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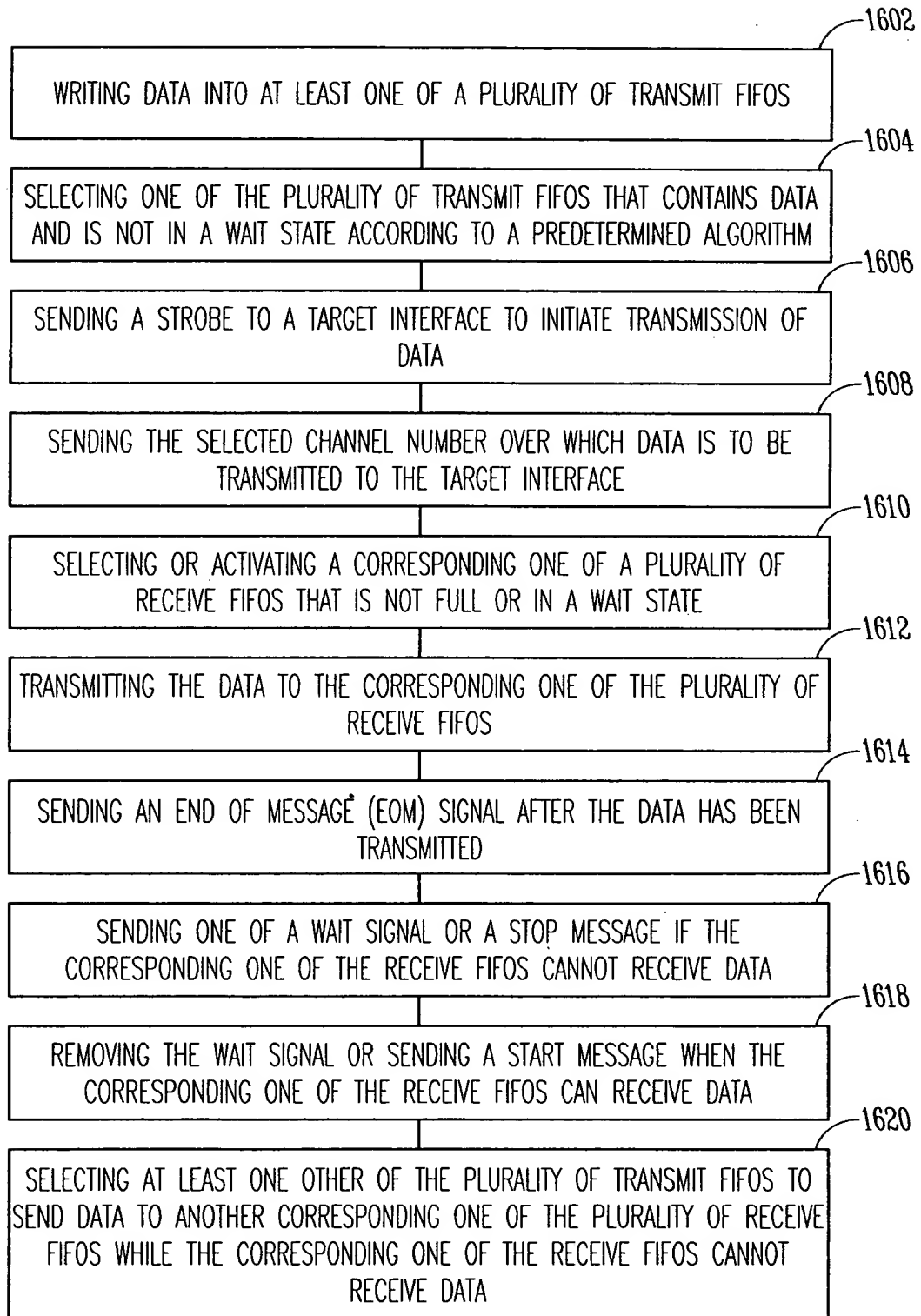


Fig.16

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